AMENDMENTS TO THE CLAIMS

1-9.(cancelled):

10.(previously presented): A computer-based communication system implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP), said system comprising:

a circuit-data-receiver to receive circuit data from a virtual container or VC-12 (SDH);

a SDH framer;

a High Order Path Adaptation function; and

a CE-to-IP function further comprising:

a packetizer to pack said circuit data into data packets;

an encapsulator to encapsulate said data packets with headers; and

a layer-2 incorporator to add layer-2 operations,

wherein said packetizer further including a packet transmit function that generates no packets when a loss of pointer is detected.

11.(previously presented): A computer-based communication system implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP), said system comprising:

a circuit-data-receiver to receive circuit data from a virtual container or VC-12 (SDH);

a SDH framer;

a High Order Path Adaptation (HPA) function; and

a CE-to-IP function further comprising:

a packetizer to pack said circuit data into data packets;

an encapsulator to encapsulate said data packets with headers; and

a layer-2 incorporator to add layer-2 operations,

wherein said packetizer further includes a packet transmit function that generates a special control packet when the HPA generates an error.

12.(previously presented): The computer-based communication system as per claim 11, wherein said packetizer further includes a packet transmit function that ignores HPA indications and transfers all data transparently.

13.(previously presented): A computer-based communication system implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP), said system comprising:

a circuit-data-receiver to receive circuit data from a virtual container or VC-12 (SDH);

a SDH framer;

a High Order Path Adaptation function; and

a CE-to-IP function further comprising:

a packetizer to pack said circuit data into data packets;

an encapsulator to encapsulate said data packets with headers; and

a layer-2 incorporator to add layer-2 operations,

wherein said packetizer further includes a packet receive function that detects loss or reception of erroneous UDP/RTP packet.

14.(previously presented): The computer-based communication system as per claim 13, wherein said erroneous UDP/RTP packet is an UDP checksum error.

15.(previously presented): A computer-based communication system implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP), said system comprising:

a circuit-data-receiver to receive circuit data from a virtual container or VC-12 (SDH);

a SDH framer;

a High Order Path Adaptation function; and

a CE-to-IP function further comprising:

a packetizer to pack said circuit data into data packets;

an encapsulator to encapsulate said data packets with headers; and

a layer-2 incorporator to add layer-2 operations,

wherein said packetizer further includes a packer receive function that detects a loss of three consecutive VC-12 frames.

16.(previously presented): A computer-based communication system implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP), said system comprising:

a circuit-data-receiver to receive circuit data from a virtual container or VC-12 (SDH);

a SDH framer;

a High Order Path Adaptation function; and

a CE-to-IP function further comprising:

a packetizer to pack said circuit data into data packets;

an encapsulator to encapsulate said data packets with headers; and

a layer-2 incorporator to add layer-2 operations,

wherein said packetizer further includes a packet receive function which outputs a AIS signal upon receipt of a control packet.

17.(previously presented): The computer-based communication system as per claim 16, wherein said packetizer further includes a packet receive function which detects error as defined in G.826.

18-22 (cancelled)

23.(currently amended): A computer-based communication system implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP) said system comprising:

a circuit-data-receiver to receive circuit data;

a CE-to-IP function further comprising:

a packetizer to pack said circuit data into data packets;

an encapsulator to encapsulate said data packets with headers; and

a layer-2 incorporator to add layer-2 operations; and

a clock-recoverer further comprising:

a receiver which receives the RTP packet;

a sampler which samples a local time stamp and a buffer pointer position;

a time-stamp-estimator which tests the sync number and calculates the estimated time stamp;

an error-calculator which calculates the error;

an inserter that inserts into array said calculated error in the right sync position according to right sync number;

a [[2T-integral-caluaitor]] 2T-integral-calculator which calculates the new integral on 2T by adding the error to the integral;

a T-integral-calculator which calculates the new integral on T by adding half of said error from said array;

a minimum-packet-comparator which maintains a continuous flow of RTP packets if minimum number of packets are reached;

a ratio-calculator that calculates the ratio of said integral on 2T and said integral on T;

a ratio-range-checker that checks to see if said ratio is between 1.5 and 3;

an angle-calculator which calculates the angle using linear regression;

a clock adjuster which adjusts clock according to said angle, and

a resetter which resets all counters, starts new windows, and start receiving RTP packets.

24-29. (cancelled)

30.(previously presented): A computer-based method implementing circuit emulation service (CE) over an Internet Protocol (IP) network (CES over IP, CESOIP), comprising the steps of:

receiving circuit data;

passing said circuit data through a CE-to-IP function, further comprising the steps of:

packing data into data packets;

encapsulating said data packets with headers; and

incorporating said data packets with layer-2 headers;

transmitting said encapsulated and layer-2 incorporated data packets via a IP network; and

passing the data packets through a clock recovery function further comprising the steps of:

receiving the RTP packet;

sampling a local time stamp and a buffer pointer position;

testing the sync number and calculating the estimated time stamp;

calculating the error;

inserting into array said calculated error in the right sync position according to right sync number;

calculating the new integral on 2T by adding the error to the integral;

calculating the new integral on T by adding half of said error from said array;

receiving RTP packets again if minimum number of packets are reached;

calculating the ratio of integral on 2T and the integral on T;

checking to see if said ratio is between 1.5 and 3;

calculating the angle by using linear regression;

adjusting clock according to said angle, and

resetting all counters, start new windows, and start receiving RTP packets.